Evolutionary Synthesis of Fractional Capacitor Using Simulated Annealing Method

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Abstract. *Synthesis of fractional capacitor using classical analog circuit synthesis method was described in [6]. The work presented in this paper is focused on synthesis of the same problem by means of evolutionary method simulated annealing. Based on a given desired characteristic function such as input impedance or transfer function, the proposed method is able to synthesize topology and values of the components in the desired analog circuit. Comparison of the results given in [6] and results obtained by the proposed method are given and discussed.*

Keywords

Simulated annealing, automated circuit synthesis, evolutionary electronics.

1. Evolutionary Electronics

Evolutionary electronics synthesis methods are able to design electronic circuits by simply directing their search towards meeting the desired specifications only. This way electronic circuits can be designed without deeper understanding their rules. Evolutionary electronics synthesis methods can also be used for problems where classical circuit synthesis methods cannot be used or do not exist. In the last two decades, a number of papers focusing on the evolutionary synthesis of electronics have been published. John Koza is the leading person of the research focused on employing genetic programming [1] where tree representation of the circuits is used. Although this method is very popular, its strong drawback is its huge computational effort. Other attempts to solve analog circuit synthesis problems were made by means of genetic algorithms (GA). J. Grimbleby has presented hybrid GA with two levels of synthesis. In the first level, topology of the circuit is selected. In the second level, values of the components are determined using numerical optimization [2]. R. Zebulum has presented three types of GA with variable length representation called OLG, ILG, UDIP [3]. A. Das and R. Vermuri have presented their method called GAPSYS which is suitable for design of passive analog circuits. Their another attempt to tackle analog circuit synthesis problem led to a method employing graph grammar based approach which is using dynamically obtained design-suitable building blocks [4]. C. Mattinusi designed its own method called AGE which is based on GA with genotype formed of alphabet of ascii letters. This method is also suitable for design of neural networks [10].

A number of different types of methods of encoding an analog electronic circuits have been published. The simplest one is the direct encoding as used by Grimbleby [2]. Its drawback is a high number of lifeless individuals produced by crossover in case of using GA [11]. This type of encoding is also used in the proposed method, however, since the crossover-free optimization method is used (simulated annealing), the problem of generation of lifeless individuals by crossover is not present in this work. Another type of encoding is developmental encoding which uses a sequence of instructions called OP codes which construct the topology of the circuit. The benefit of using of this method is low number of unsimulatable circuits generated by crossover. On the other hand there can be restriction of the circuit topologies which can be encoded using this method. Developmental encoding was used for example in [12] or [13]. Description of the analog circuit using adjacent matrix have been presented by Mesquita [11]. The principle is to represent analog circuit topology as a graph which is defined by a 2-dimensional matrix. For the purpose of crossing, this matrix is transformed into rows and special crossover is used. The use of this method for design of antenna matching network was presented in [14].

With progress in evolutionary techniques, new evolutionary methods are employed in the field of evolutionary electronics. Zinchenko has presented several papers describing synthesis of analog electronics employing univariate marginal distribution algorithm (UMDA). For example, synthesis of mixed analog-digital circuits was presented in [15]. UMDA was also used in [13] where the algorithm determines the numbers of capacitors, resistors and inductors in the analog circuit.

The presented work is focused on evolutionary synthesis of analog electronic circuits by means of pure simulated annealing algorithm. This method was used in ASTRX/OBLS [16] however the systems were targeted to synthesis of sizing of the analog circuit only. The presented method is focused on synthesis of both the topology and also the values of the components.

2. Synthesis of Analog Electronics by Means of Simulated Annealing

Simulated annealing (SA) is a method of global optimization which is able to find the minimum of a given search space [5]. Its best feature is the ability of not getting stuck in local optima of a complicated search space. Unlike for some other global optimization methods, a proof of statistical convergence of SA can be made [17]. Flow chart of the simulated annealing algorithm as used in the proposed method is presented below as Algorithm 1.

Algorithm 1 Simulated annealing

```
1: k ← 0, randInit(e)
2: while T > T_f do
3:     T ← temp(k, T_0, r)
4:     δx ← rand{−1, 1}
5:     e_n ← e, e_n(i) ← e_n(i) + δx
6:     Δ_c ← (c(e_n)−c(e))
7:     if P_a(T,Δ_c) >rand then
8:         e ← e_n
9:     end if
10:    k ← k + 1
11: end while
```

As you can see in Algorithm 1, the first step of SA is initialization of counter k and solution e which is set randomly. Thereafter the main iteration loop begins. In every iteration, temperature T is calculated according to an exponential cooling scheme given by (1) [5].

$$T = T_0.exp(-r.k). \tag{1}$$

The coefficient r defines the speed of cooling. In the next step, neighborhood e_n of the actual state e is generated. Variable of solution e is randomly chosen and its value is, based on the result of random generator, increased or decreased by 1. After evaluation of the cost of neighborhood $c(e_n)$, difference of cost of neighborhood and cost of old state can be computed. According to (2), neighborhood e_n is accepted as the new state e or not,

$$P_a = \frac{1}{(1+exp(\Delta/T)}. \tag{2}$$

While the current temperature T is decreasing, the described process is repeated until T reaches the defined final temperature T_f.

For encoding analog circuit topology and values of the components, a simple direct representation was used [2], [11]. As mentioned in the introduction, this encoding method is not very suitable for use with genetic algorithms where its crossover produces a high number of unsimulatable circuit topologies. Nevertheless, since we use crossover-free optimization method, this method of encoding is sufficient for our purpose. Direct encoding method will be described in the text bellow.

Encoding string e is formed of n integer numbers. For passive circuits, every component of the circuit is defined by a sequence of 5 integer variables. Therefore the maximal complexity of encoded circuit is $n/5$.

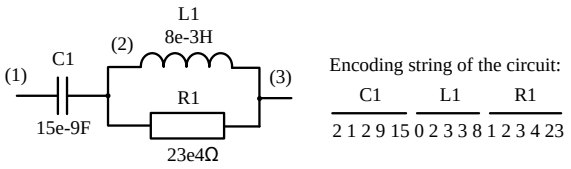

Fig. 1. a) Example of analog circuit, b) its encoding string.

Every component of the encoded circuit is described by a sequence of 5 integer variables defining its type, connection node 1, connection node 2, exponent (*exp*) and mantisa (*man*). Definition of types of components is: 0 - L, 1 - R, 2 - C. Numbers (1), (2), (3) in the schematic in Fig. 1a denote the names of the nodes. For example capacitor C1 which is connected to nodes 1 and 2 is defined by sequence 2 1 2 9 15 (first five numbers in the encoding string in Fig. 1b). Its value can be computed as $C1 = man.10^{p.exp}$, where $p = -1$ for capacitors, $exp = 9$ and $man = 15$. This way other components of the circuit in Fig. 1a can be encoded. The method allows encoding of all kinds of electrical components as for example transistors or operational amplifiers.

The cost of the circuit $c(e_n)$ defined by encoding string e_n is computed using (5) which is a weighted summation of deviations in magnitude and phase responses of the actual solution. Deviation of magnitude Δ_m is computed as summation of differences of desired magnitude characteristic f_{dm} and magnitude of actual solution f_{am} over m frequency points (see (3)). Deviation of phase Δ_p is computed as a summation of differences of the desired phase characteristic f_{dp} and phase of actual solution f_{ap} (see (4)).

$$\Delta_m = \sum_{i=1}^{m} (f_{dm}(i) - f_{am}(i))^2, \tag{3}$$

$$\Delta_p = \sum_{i=1}^{m} (f_{dp}(i) - f_{ap}(i))^2, \tag{4}$$

$$cost = \Delta_m w_m + \Delta_p w_p. \tag{5}$$

Experiments have shown that the deviation of magnitude Δ_m in (5) is not necessary however it helps the search process to be guided towards the desired solution. Responses of the encoded circuits are computed using nodal analysis in Matlab. Since ideal resistors, capacitors and inductors are used the nodal analysis consists only in construction of admittance matrices for all frequency points and calculation of its determinants. Approximate duration of one simulation is 5 ms. If there is a requirement of different circuit components than passive RLC only, external circuit simulator has to be used. The cost evaluation is then formed from two steps. The first one is generating of netlist file. The second one is simulation using a spice-compatible circuit simulator (HSPICE, NGSPICE). The simulator allows to employ a wide variety of types of the components and circuit analysis methods. On the other hand, the time of single simulation increases to tens of ms. For numbers of cost function evaluations like 1e6, this time is very significant.

3. Design of Fractional Capacitor Using Classical Method of Synthesis

Authors of [6] describe approximation of fractional capacitors $(1/s)^{1/n}$ by a regular Newton process and they present its RLC network representations which are obtained using a classical method of analog circuit synthesis. Synthesis of the fractional order systems is discussed also in [7], [8], [9], [21]. The problem of synthesis of the circuit approximation of (6) was adopted from the mentioned paper and will be used for demonstration of synthesis capabilities of the proposed method. In [6] function (6) was approximated by 5$^{\text{th}}$ order function (7) which was obtained using symbolic analyzer SNAP [20].

$$Z_{in} = s^{-0.6} \tag{6}$$

$$Z_{in} = \frac{8.58s^4 + 255s^3 + 405s^2 + }{1s^5 + 94.2s^4 + 472s^3 + } \cdots$$
$$\cdots \frac{+35.9s + 0.169}{+134.8s^2 + 2.627s + 9.8.10^{-3}} \tag{7}$$

In Fig. 2 the realization of function (6) is shown as presented in [6]. For the rest of the paper, the circuit will be called "original approximation circuit".

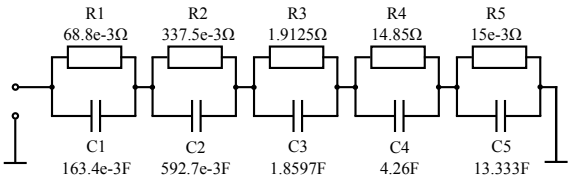

Fig. 2. Schematic of the original approximation circuit.

Comparison of magnitude of Z_{in} of original approximation circuit and function (6) is presented in Fig. 3. The broken line represents function (6), the solid line represents original approximation circuit. Since the deviation is not clear from the picture, absolute value of difference of both curves plotted in Fig. 3 is presented in Fig. 4.

Deviations of magnitude of Z_{in} of original approximation circuit at borders and inside of the used frequency range are summarized in Tab. 1.

$\omega[rad/s]$	0.01	100	0.3311
$\Delta_{mag}[dB]$	0.71	0.46	0.61

Tab. 1. Maximal magnitude deviations of Z_{in} of the original approximation circuit.

The phase characteristic of Z_{in} of the original approximation circuit is presented in Fig. 5. As in the case of magnitude of Z_{in}, Fig. 6 presents absolute values of differences between curves in Fig. 5.

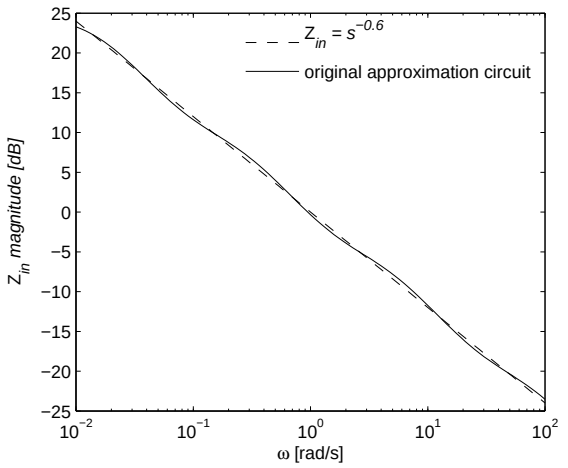

Fig. 3. Comparison of magnitude of Z_{in} of the original approximation circuit and ideal function (6).

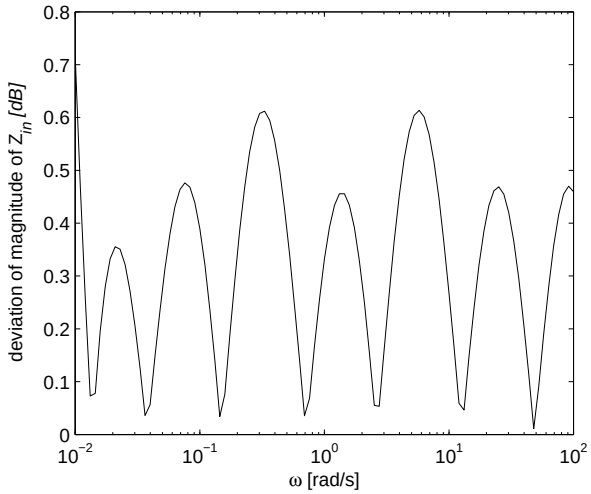

Fig. 4. Deviation of magnitude of Z_{in} of the original approximation circuit.

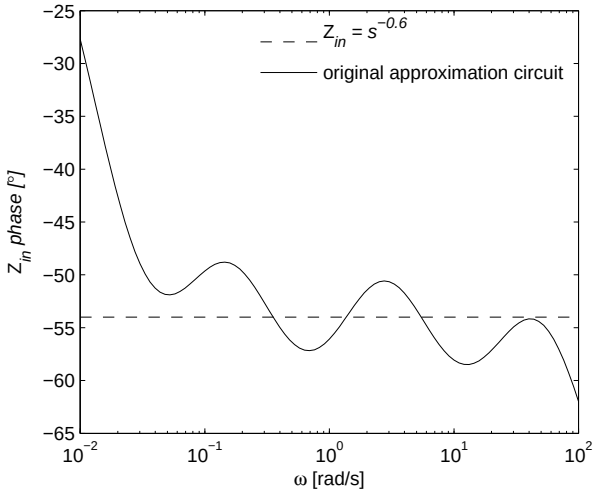

Fig. 5. Comparison of phase of Z_{in} of the original approximation circuit and ideal function (6).

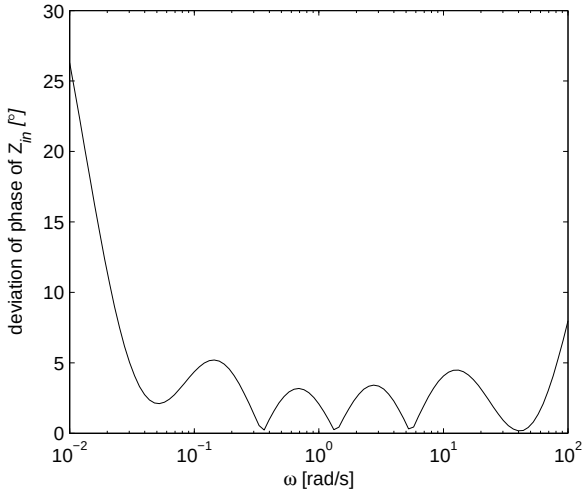

Fig. 6. Phase deviation of Z_{in} of the original approximation circuit.

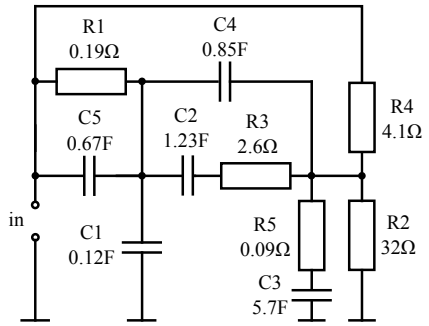

Fig. 7. Schematic of the best found solution.

$\omega[rad/s]$	0.01	100	0.14
$\Delta_{phas}[\circ]$	26.3	7.98	5.2

Tab. 2. Maximal phase deviations of Z_{in} of the original approximation circuit.

Highest deviations of ideal function (6) and phase response of original approximation circuit are summarized in Tab. 2.

4. Solution of the Proposed Method

The goal of the synthesis is to design a circuit which approximates the function (6). The only informations supplied to the synthesis system are the desired magnitude and phase characteristics of (6) and the maximal number of used components which was set to 10. The number was chosen to use the same maximal circuit complexity as the original approximation circuit. The synthesis method is set to use resistors, capacitors and inductors only. The constrains of values of the components were set to allow the optimization to reach the same components values as presented in the paper [6]. Since the used angular frequency range is from 0.01 rad/s to 100 rad/s, the values of the components are set to non-realistic values. The maximal ranges of values of all the three types of components (RLC) were set to 10^{-4} to 10^5. Note that the values of resistors can also be negative.

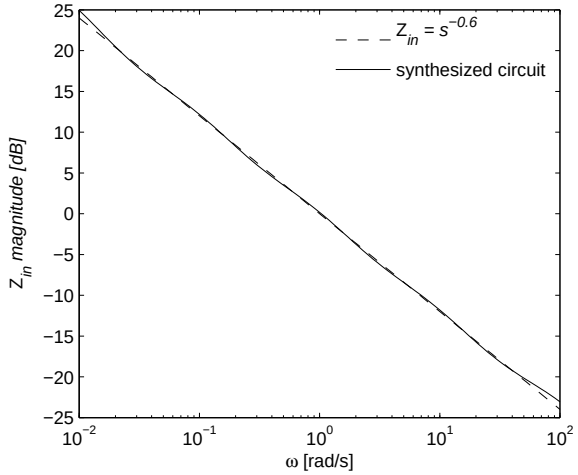

Fig. 8. Comparison of magnitude of Z_{in} of the synthesized circuit and desired function (6).

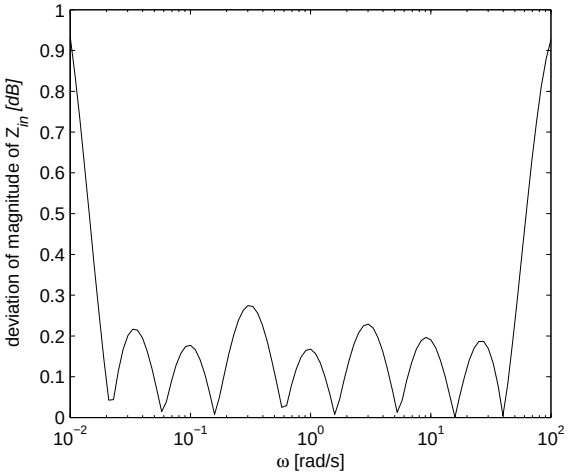

Fig. 9. Magnitude deviation of Z_{in} of the synthesized circuit.

initial temperature	T_0	6000
cooling coefficient	r	7.10^{-5}
final temperature	T_f	3.10^{-10}
number of variables	n	50
number of frequency points	m	101
magnitude weigth	w_m	1
phase weigth	w_p	2

Tab. 3. Parameters of the optimization method.

For the synthesis of the problem 440.10^3 cost function evaluations were used and the synthesis took 80 min on a standard PC (Intel Core2 6420@2GHz, 1GB RAM). 20 instances of the simulated annealing algorithm were executed. Cost value of the best found circuit was $cost = 2.4537$ ($\Delta_m = 0.2419$ and $\Delta_p = 1.1059$). Its schematic is presented in Fig 7.

The magnitude response is given in Fig. 8. Absolute value of deviation of the magnitude is presented in Fig. 9.

As can be seen in Fig. 9 the maximal errors of the magnitude response were at the borders of the used frequency range. At these frequencies the response of the circuit neighborhoods with the unoptimized areas of the circuit behavior

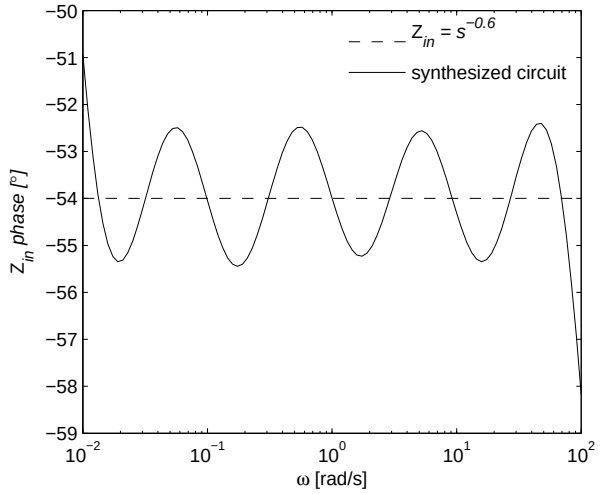

Fig. 10. Comparison of phase of Z_{in} of the synthesized circuit and the desired function (6).

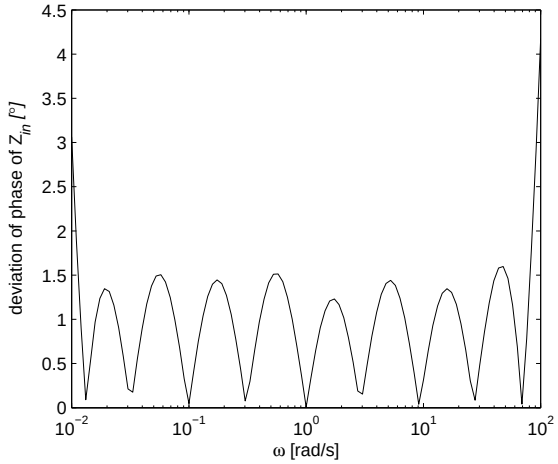

Fig. 11. Phase deviation of Z_{in} of the synthesized circuit.

and it affects the response of the circuit in the range where it is optimized. Three highest deviations in the magnitude of Z_{in} of the synthesized circuit are presented in Tab. 4.

$\omega[rad/s]$	0.01	100	0.30
$\Delta_{mag}[dB]$	0.93	0.92	0.27

Tab. 4. Deviations of magnitude of Z_{in} for the synthesized circuit.

Phase response of the synthesized circuit is presented in Fig. 10. The absolute value of difference of these curves is presented in Fig 11.

Three highest deviations of the phase characteristic at the borders and inside the used frequency range are presented in Tab. 5.

$\omega[rad/s]$	0.01	100	0.58
$\Delta_{phas}[\circ]$	3	4.2	1.5

Tab. 5. Deviations of phase of Z_{in} for the synthesized circuit.

Zeros and poles diagram of the synthesized circuit is presented in Fig. 12.

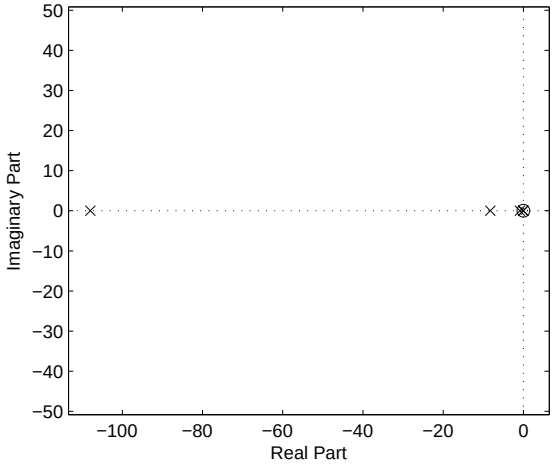

Fig. 12. Zeros and poles diagram.

In the text bellow the original approximation circuit and the circuit obtained using the proposed method will be compared. Comparison of the deviations of magnitude of Z_{in} for both circuits is presented in Tab. 6.

original circuit	$\omega[rad/s]$	0.01	100	0.33
	$\Delta_{mag}[dB]$	0.71	0.46	0.61
synthesized circuit	$\omega[rad/s]$	0.01	100	0.30
	$\Delta_{mag}[dB]$	0.93	0.92	0.27

Tab. 6. Comparison of deviations of magnitude of Z_{in} for the original and the synthesized circuit.

Except deviations at boundaries of the used frequency range (as commented above) the highest deviation in the used frequency range for the original approximation circuit is $\Delta_{mag} = 0.61$ dB at angular frequency 0.33 rad/s. For the solution of the proposed method, the highest deviation of the magnitude is $\Delta_{mag} = 0.27$ dB at angular frequency 0.30 rad/s. Thus the terms of deviation in magnitude the accuracy of the synthesized circuit is more than two times better than the original approximation circuit. Note that the number of components is the same for both circuits. Comparison of maximal deviations of phase of Z_{in} is presented in Tab 7.

original circuit	$\omega[rad/s]$	0.01	100	0.14
	$\Delta_{phas}[\circ]$	26.3	7.98	5.2
synthesized circuit	$\omega[rad/s]$	0.01	100	0.58
	$\Delta_{phas}[\circ]$	3.0	4.2	1.5

Tab. 7. Comparison of deviations of phase of Z_{in} for original and synthesized circuit.

As in the case of magnitude Z_{in}, deviation of phase is also highest at the borders of the used frequency range for both circuits. The highest phase deviation inside the used frequency range for the original circuit is $\Delta_{phas} = 5.2^\circ$ at angular frequency 0.14 rad/s and for the synthesized circuit it is $\Delta_{phas} = 1.5^\circ$ at angular frequency 0.58 rad/s. Thus phase accuracy of the synthesized circuit is more than three times better than the original approximation circuit.

Although the probability of using of the all three component types (resistors, capacitors, inductors) was equal during the synthesis process, the synthesized circuit does not include any inductors (see Fig. 7). As the synthesis method was constrained to use maximally 10 components, it seems that using only capacitors and resistors allows the method to reach a lower cost value than in the case of solutions where also inductors are included.

The synthesis of approximation circuit with desired input impedance characteristic was presented. The problem was chosen for comparison of the new proposed method of synthesis to classic analog circuit synthesis method. Although the problem was formulated as synthesis of analog network with desired input impedance (one-port network), the problem can be easily formulated as searching for the analog network with desired transfer function (7) (two-port network).

5. Experimental Verification

Since the frequency range and values of the components of the synthesized approximation circuit (Fig. 7) are rather theoretical than practical, a simple method will be presented for transformation of the synthesized approximation circuit to frequency range and values of the components which are more suitable for practical realization.

The transformation is very simple. Let's define transformation coefficients k_r and k_c which denote transformation of values of resistors and capacitors respectively. Transformed value R_i' of resistor R_i can be obtained as $R_i' = k_r R_i$. Similarly the transformed value C_i' of capacitor C_i can be obtained as $C_i' = k_c C_i$. The values of coefficients k_r and k_c are chosen to meet the desired frequency range and to obtain feasible values of the components. For the purpose of the experimental verification the angular frequency range was transformed to ω_1=100 rad/s, $\omega_2 = 1.10^6$ rad/s which corresponds to frequency range f_1=15.9 Hz, f_2= 159 kHz. Values of the components were transformed to the range which allows easy implementation of the synthesized circuit at experimental board using passive components of standard E24 series. The transformation coefficients were set to $k_r = 1.10^3$ and $k_c = 1.10^{-7}$. Values of the components before and after the transformation are presented in Tab. 8 and Tab. 9 respectively.

Magnitude and phase characteristics of the transformed approximation circuit are presented in Fig. 13 and Fig. 14 respectively. Note that the transformation which was described above introduces a multiplier constant to (7). The constant can be represented as additional voltage gain. In Fig. 13 the multiplier constant causes shifting of the magnitude of Z_{in} 60 dB upwards (compare Fig. 13 to Fig. 8). Note that the phase characteristic is not influenced.

The measurement was performed using automatic impedance measurement system based on Agilent VEE software and devices Agilent 33220A and Agilent 54621A. See [22] for more details. Comparison of the magnitude characteristics of the simulated and the measured circuit is presented in Fig. 15. Absolute value of difference of these two characteristics is presented in Fig. 16.

Similarly comparison of the phase characteristics of the simulated and the measured circuits is presented in Fig. 17. Its difference is presented in Fig. 18.

R1	R2	R3	R4	R5
0.19 Ω	32 Ω	2.6 Ω	4.1 Ω	0.09 Ω
C1	C2	C3	C4	C5
0.12 F	1.23 F	5.7 F	0.85 F	0.67 F

Tab. 8. Values of the components before the transformation.

R1	R2	R3	R4	R5
190 Ω	32 kΩ	2.6 kΩ	4.1 kΩ	90 Ω
C1	C2	C3	C4	C5
12 nF	123 nF	570 nF	85 nF	67 nF

Tab. 9. Values of the components after the transformation.

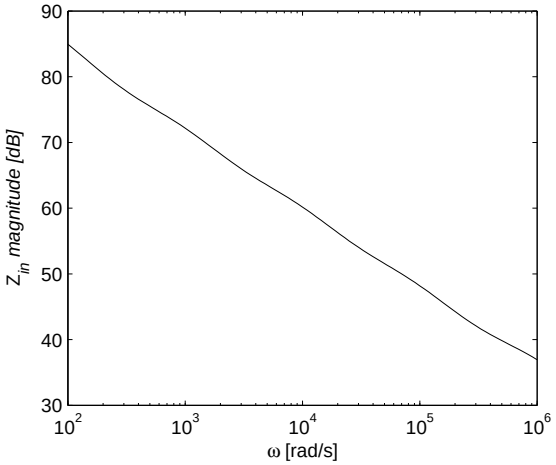

Fig. 13. Magnitude characteristic of Z_{in} of the transformed circuit.

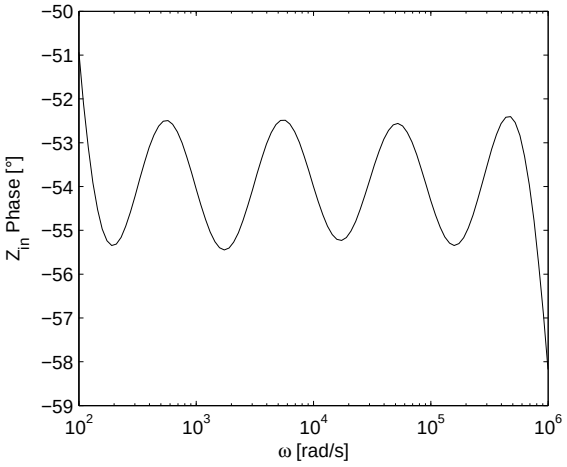

Fig. 14. Phase characteristic of Z_{in} of the transformed circuit.

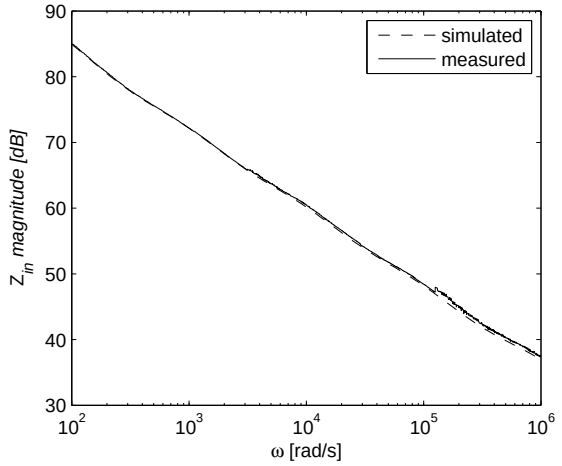

Fig. 15. Comparison of magnitude characteristics for the measurement and the simulation.

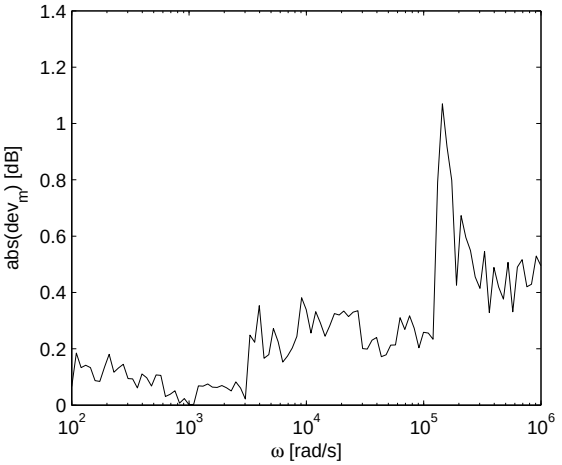

Fig. 16. Magnitude deviation of the measured circuit.

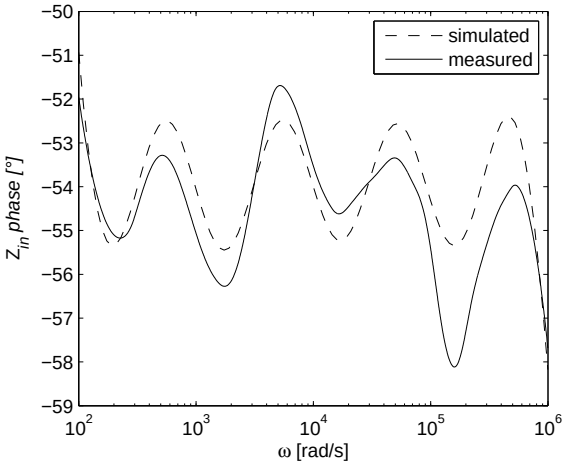

Fig. 17. Comparison of phase characteristics for the measurement and the simulation.

As can be seen in Fig. 15 to Fig. 18 the highest deviations of the measured and the simulated circuits are for $\omega = 144,5.10^3$ rad/s. The deviations are $\Delta_m = 1.07$dB for magnitude (Fig. 16) and $\Delta_p = 2.652^\circ$ for phase (Fig. 18).

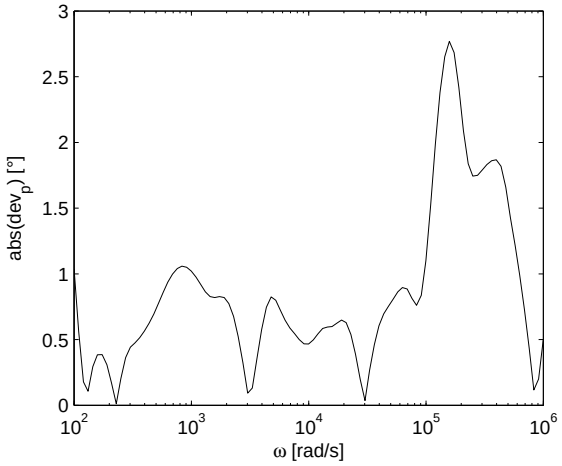

Fig. 18. Phase deviation of the measured circuit.

There are two main reasons for the deviation between the simulated and the measured responses. The first one is that the components of the realized circuit were chosen from E24 series. This selection causes lower precision of the values of the used components and therefore the approximation function (7) is not fully accomplished. The second reason is worse performance of the used experimental board at higher frequencies however since the highest used angular frequency was 1.10^6 rad/s (159 kHz), the frequency influence of the experimental board should be negligible.

The main aim of the measurement was experimental verification of the proposed synthesized circuit what was accomplished. The measurement has shown that even for lower precision realization of the synthesized circuit (using components of standard E24 series), magnitude and phase responses with acceptable deviations can be obtained.

6. Conclusion

Evolutionary electronics synthesized method based on the simulated annealing global optimization method was proposed. Synthesis ability of the method was verified on the synthesis problem of a fractional capacitor circuit adopted from [6]. The proposed method was configured to use the same maximal circuit complexity (and therefore also the same order of the approximation function) as the original approximation circuit presented in [6]. Experiment has shown that the proposed method is able to reach better accuracy than classical method of analog circuit synthesis. For the given desired fractional order system $Z_{in} = s^{-0.6}$ the proposed method was able to synthesize topology and values of the components of the approximation circuit. The maximal deviations of the best circuit which was found by the proposed synthesis method were $\Delta_m = 0.27$ dB and $\Delta_p = 1.5^\circ$. Maximal magnitude deviation of the synthesized circuit was more than two times lower than the original approximation circuit. Maximal phase deviation was more than three times lower. The discovered network can be used for synthesis of chaotic circuits with fractional dimension. The systematic design procedure for autonomous chaotic systems can be found in [18] and for driven dynamics in [19].

Acknowledgements

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